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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
KW	5,513,135	04/30/1996	Dell et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

KW (1)	"Intel 82804AA Memory Repeater Hub for SDRAM (MRH-S) Datasheet", Intel Corp., pp. 2-48, (Nov 1999)
KW (2)	"Intel 82805AA Memory Translater Hub (MTH) Datasheet", Intel Corp., pp. 1-48, (Nov 99)
KW (3)	A. Cataldo "TI fields DSP-Based Media Processor on a DIMM" , EE Times (Jan., 2000)
KW (4)	P. Mac Williams, "PC Memory Directions For 1999 and Beyond", Intel Developer Forum, pp. 1-10, (Sept. 1998)
KW (5)	B Johnson, "Direct RDRAM Basic Architecture and Program Overview", Intel Developer Forum, pp. 1-14, (Sept. 1998)
KW (6)	P. Gillingham, "SLDRAM Architectural and Functional Overview", SLDRAM Consortium, SLDRAM Inc., pp. 1-14 (Aug. 1997)
KW (7)	" Draft Standard For a High-Speed Memory Interface (Synclink) ", Draft 0.99 IEEE P1596.7-199X, IEEE Inc. (1996), pp. 1-51
KW (8)	"KMM377S1620CT2 SDRAM Module Datasheet", Samsung Electronics Inc., pp. 1-2, (Nov. 98)
KW (9)	"SLD4M18DR400 4MEG x 18 SLDRAM Datasheet", SLDRAM Inc.. pp. 1-69, (July 98)
KW (10)	J. Poulton, "Signaling in High Performance Memory Systems", IEEE Solid State Circuits Conference, slides 1-59, (Feb. 1999)

EXAMINER Kevin Verbrugge	DATE CONSIDERED 1/3/02

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.